ARM Next-Generation IP Supporting Avago High-End Networking

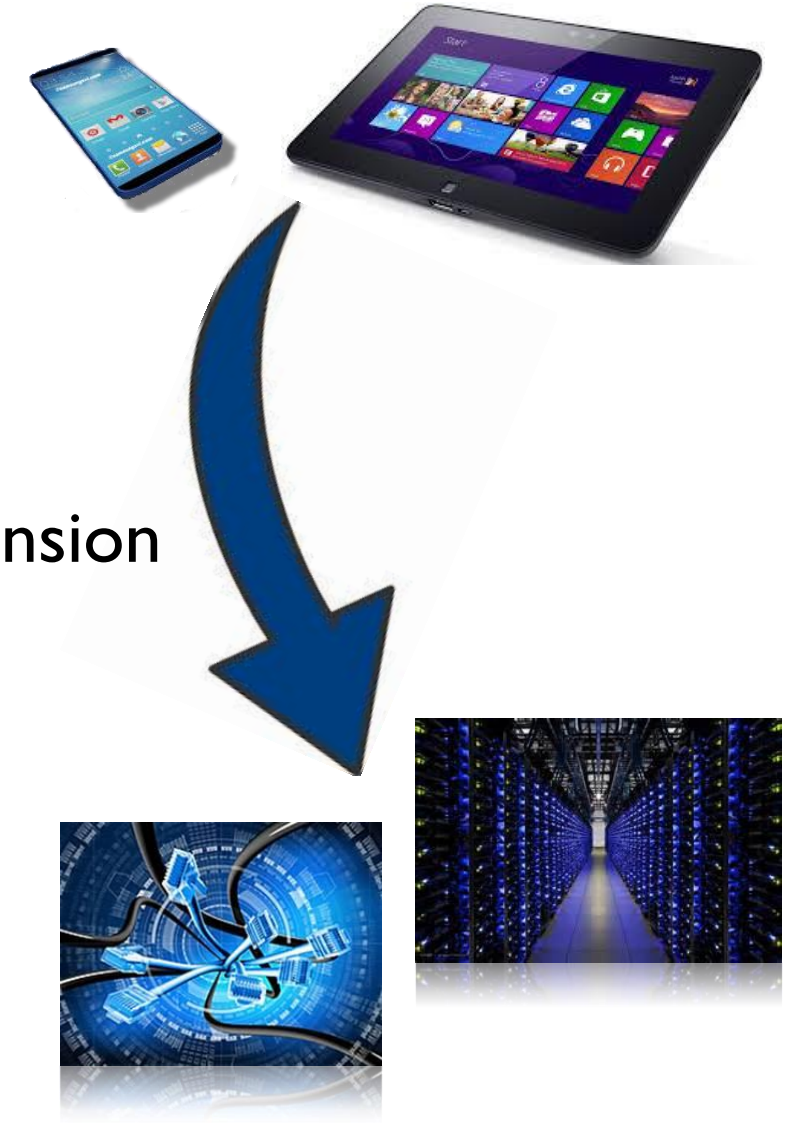
Mike Filippo – ARM® Lead Architect
David Sonnier – Avago Technologies® Lead Architect

Agenda

- ARM next-generation 64-bit CPU IP
- ARM enterprise system IP
- Avago Axxia® communication processor platform architecture
- Axxia 5516
- Axxia software
- Axxia advantages for networking applications

ARM Expansion Into Enterprise

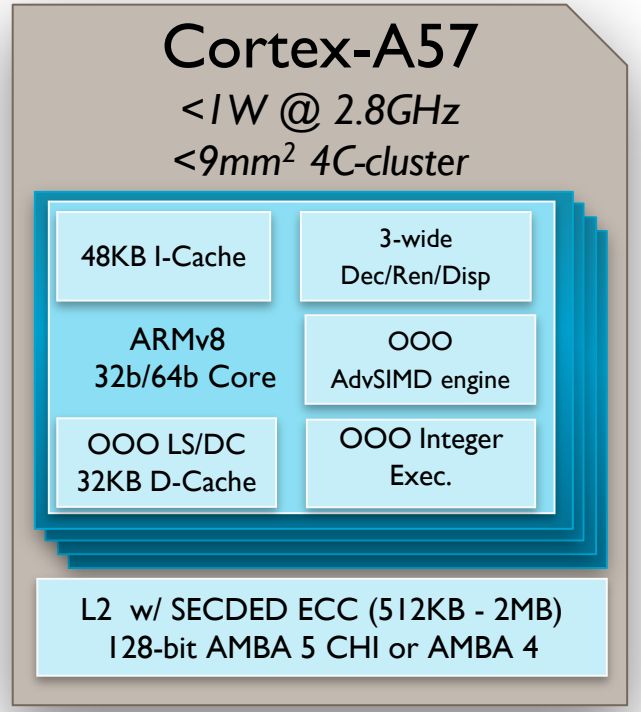
- ARM has historically focused on the mobile market
- Our ecosystem and performance/power-efficiency is enabling a significant move into the enterprise space
- A number of new products enabling enterprise expansion
  - CPUs – Cortex® -A57 / Cortex-A53
  - Scalable interconnects – CoreLink CCN-508 / CCN-504
  - Architectures – ARMv8-A, AMBA® 5 CHI
- Performance, power-efficiency, scalability
  - A new generation of IP enabling order-of-magnitude scaling



AVAGO TECHNOLOGIES

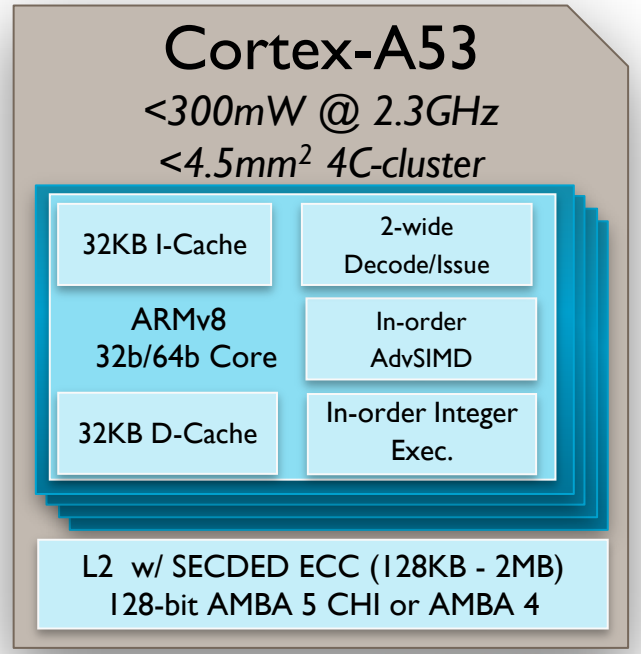
ARM

Cortex-A57/A53: A Continuum of Performance/Power



- **Cortex-A57: ARM's highest-performance 64-bit CPU**
- 3-wide dispatch, 8-wide out-of-order issue, 128 in-flight instructions
- 48K I$, 32K D$, shared L2 cache (512KB-2M, 16-way)

- **Cortex-A53: ARM's most power-efficient 64-bit CPU**
- In-order, dual-issue superscalar execution
- 32K I$, 32K D$, shared L2 cache (128KB-2M, 8-way)

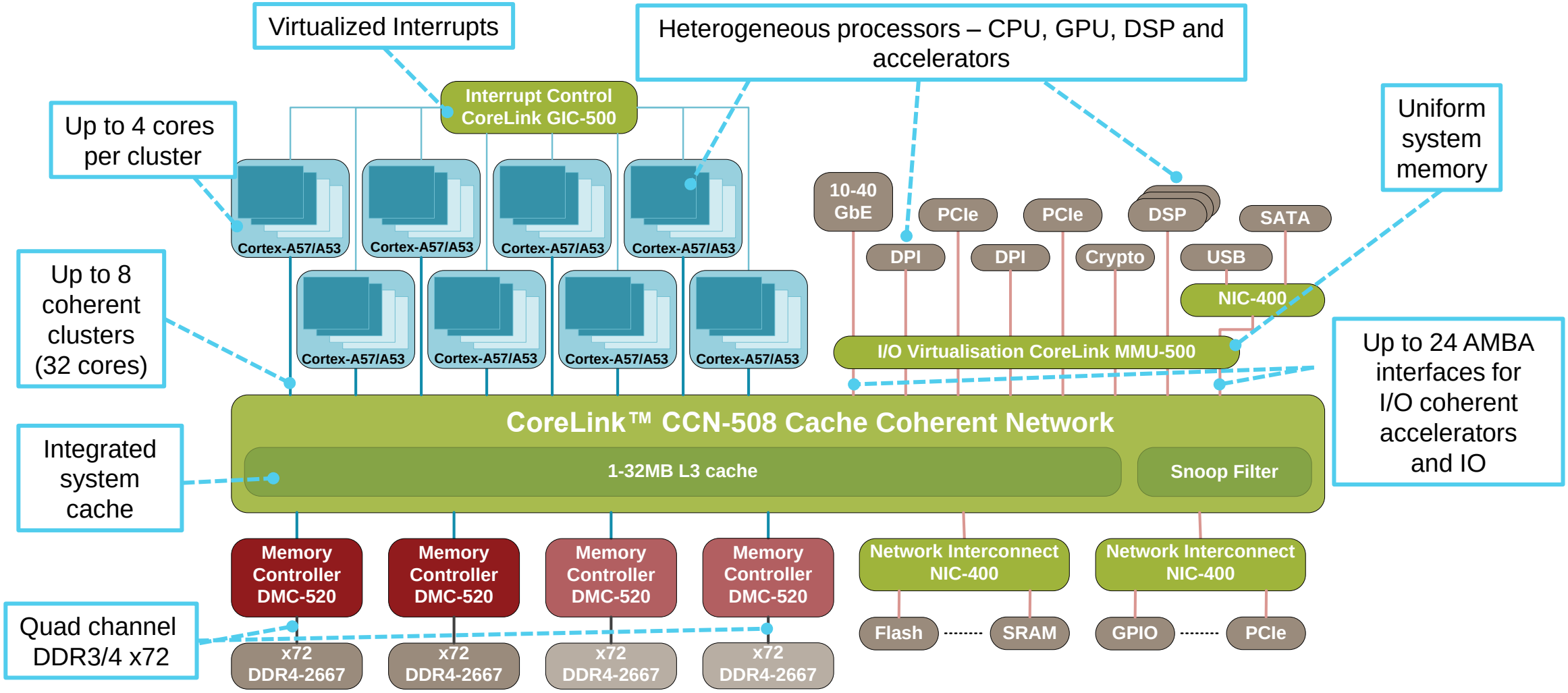


Co-optimized perf/power continuity enabling big.LITTLE™ multiprocessing

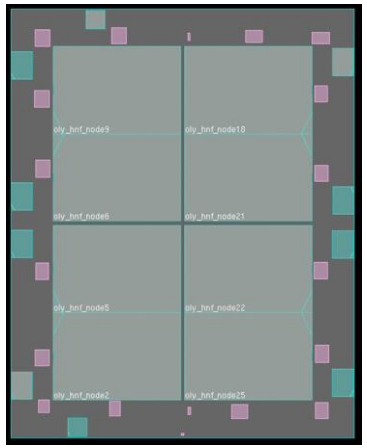
AVAGO TECHNOLOGIES

ARM

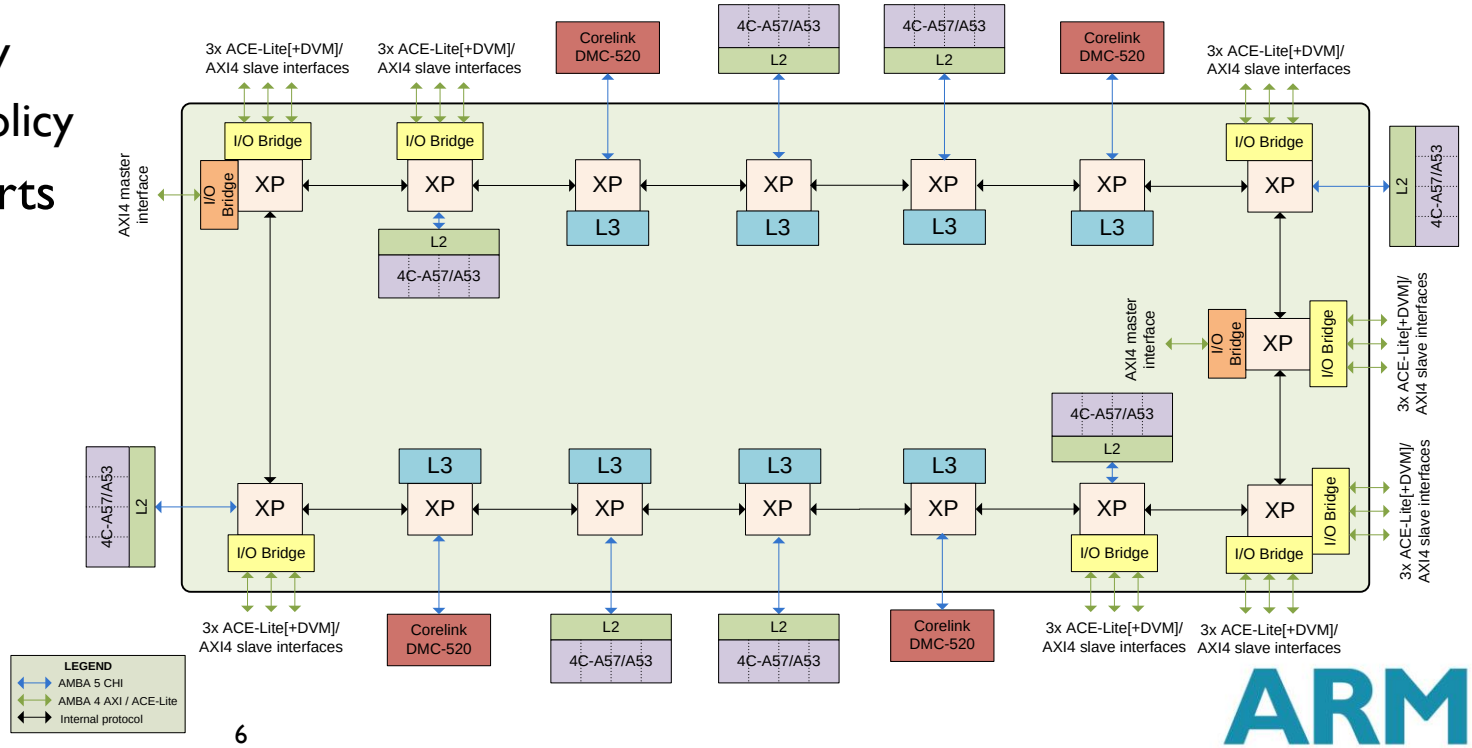
ARM CoreLink System IP



CoreLink CCN-508 System Architecture



- 8x processor clusters (32-CPU system), 4 25GB/s memory-controller ports
- Transport Layer – fully distributed, implementation-aware design
  - Core-frequency, single-cycle transport - five bi-directional rings supporting AMBA 5 CHI virtual channels
  - 4x128-bit data rings - 2.9Tbps peak, 1.8Tbps sustained throughput
- L3 + PoC/PoS + Snoop-filter: 8x partitions, 1M-32M total capacity
  - Ordering/coherency point(s) for accesses to DRAM
  - Snoop-filtering for coherency scalability
  - Adaptive exclusion/inclusion caching policy
- 8x I/O-master bridges – 24 ACE-Lite ports
  - I/O coherent w/ SMMU support
  - 320+Gbps usable bandwidth / bridge
  - Uses L3 for flexible I/O caching
- Integrated system-clocking support
  - Source-synchronous async bridges
  - Flexible clock-ratios, timing-mitigation



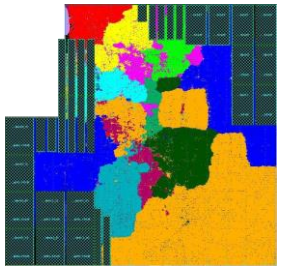
CoreLink CCN-508 QoS / Power-Management Architecture

- End-to-end QoS from ingress to egress and throughout interconnect
- Optional QoS regulation at all ingress points
  - User sets latency/bandwidth requirements, QoS-requirements produced accordingly
  - Regulate for guaranteed latency, minimum latency, available bandwidth
- Prioritized arbitration and elimination of head-of-line blocking at:
  - Ring upload/download, I/O-bridge ingress/arbiter/scheduler, L3 scheduler/retry-protocol
- QoS-based, hybrid-retry protocol-layer flow-control (AMBA 5 CHI)

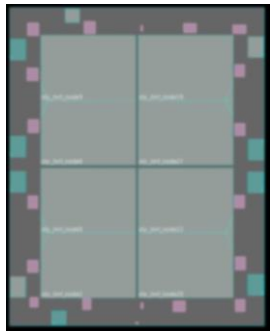
- L3 partial power-down
  - Power-down half of the L3 data/tag RAMs (16-way → 8-way, snoop-filter remains active)
- L3 RAM power-down
  - Power-down all of L3 data/tag RAMs when caching not needed (snoop-filter remains active)
- L3 active retention
  - L3 RAM retention control w/ in-pipeline wake-up

ARM IP Enabling Enterprise Solutions

- Next-generation ARM IP is pushing the envelope of compute and system scalability
  - Cortex-A57 / Cortx-A53 CPUs offer high performance and extreme power efficiency to satisfy enterprise compute requirements
  - Corelink CCN-504/CCN-508 enable highly scalable system solutions with 16-core and 32-core form-factors



- But in the end, the ARM ecosystem is all about our partners and their ability to use ARM IP to help create new and innovative products
  - Illustrated by our close working relationship with Avago in enterprise networking



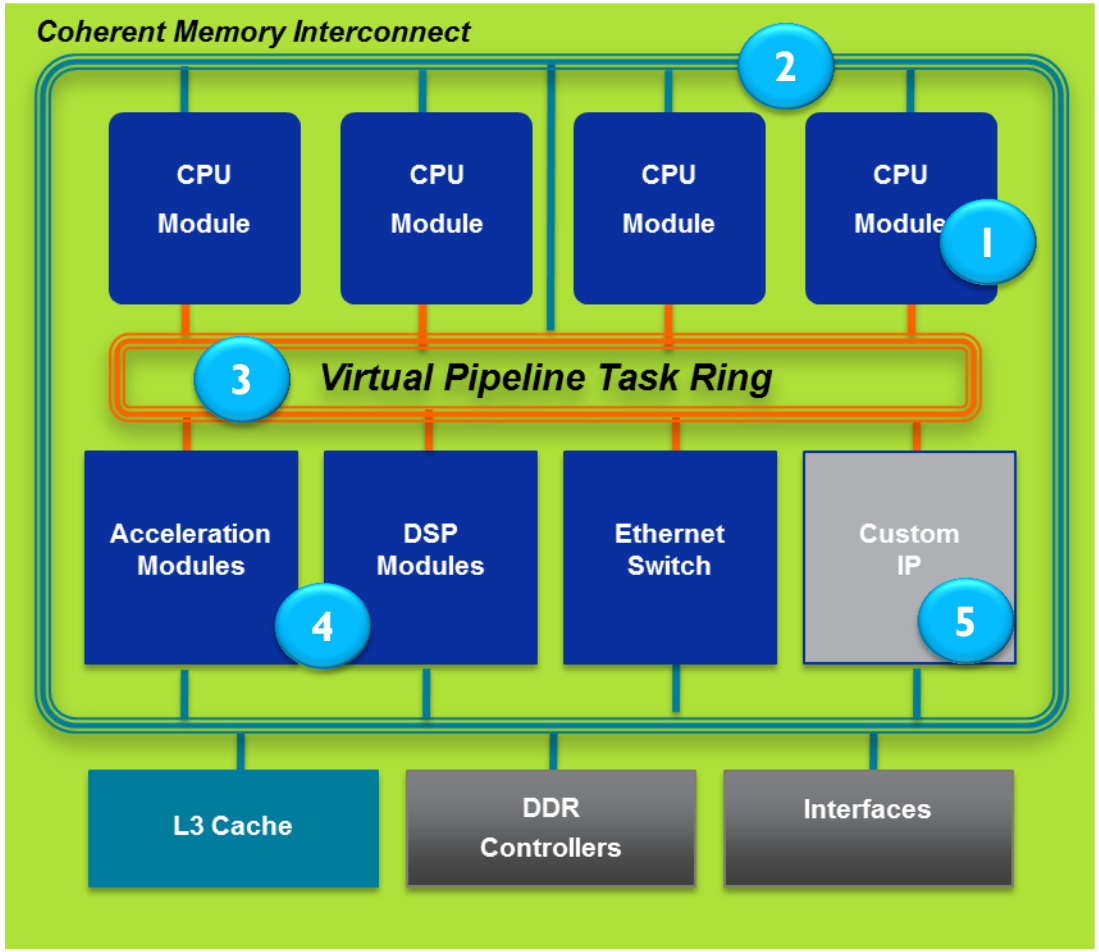
AVAGO TECHNOLOGIES

ARM

Agenda

- Avago Axxia Platform Architecture
- Axxia 5516
- Axxia Software
- Axxia Advantages for Networking Applications

Avago Axxia Platform Architecture



Turn-Key Software

Key Architectural Elements

1. High Performance Low Power Cores
2. Low Latency, QoS Aware Multicore Interconnect
3. Virtual Pipeline Autonomous Processing
4. Market Leading Acceleration Engines
5. Flexible Integration of 3rd Party & OEM IP blocks

Axxia accelerates performance & increases power efficiency

Axxia Acceleration Model Comparison

Need packet flow through engine 1, engine 3, CPU, engine 2 and then out.

Non-Pipelined

- Wastes CPUs to chain acceleration engines

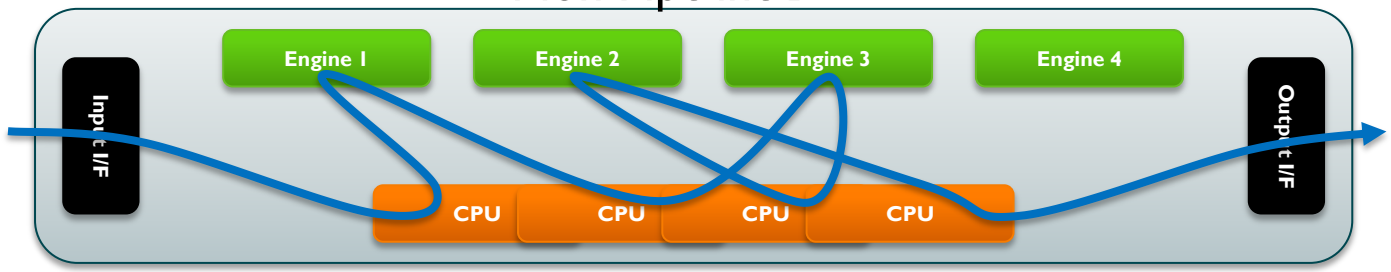
Fixed Pipeline

- Not flexible enough to support this ordering without going through engines twice

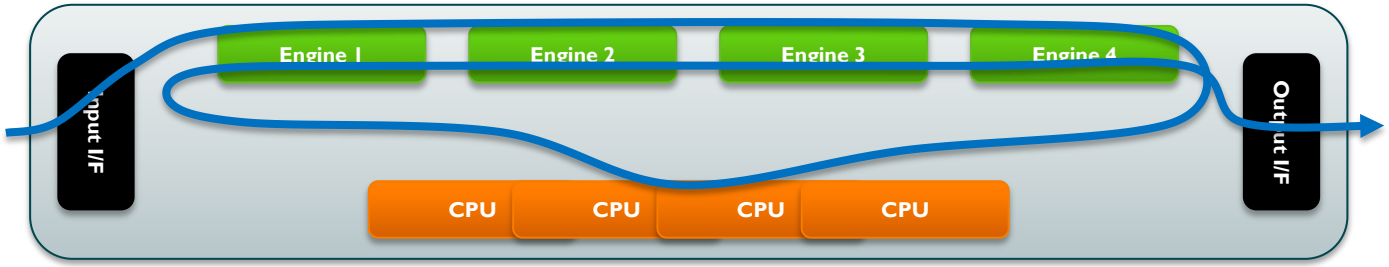
Virtual Pipeline

- Use acceleration engines in any order
- Each packet can run on a different pipeline

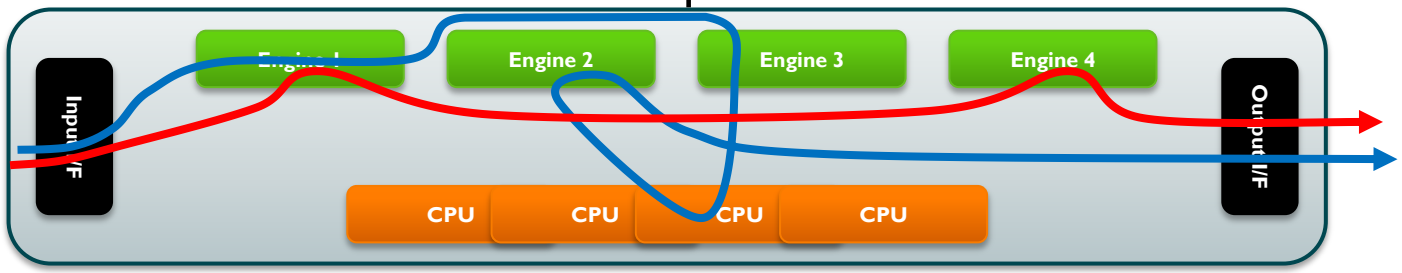
Non Pipelined



Fixed Pipeline



AVAGO TECHNOLOGIES Virtual Pipeline



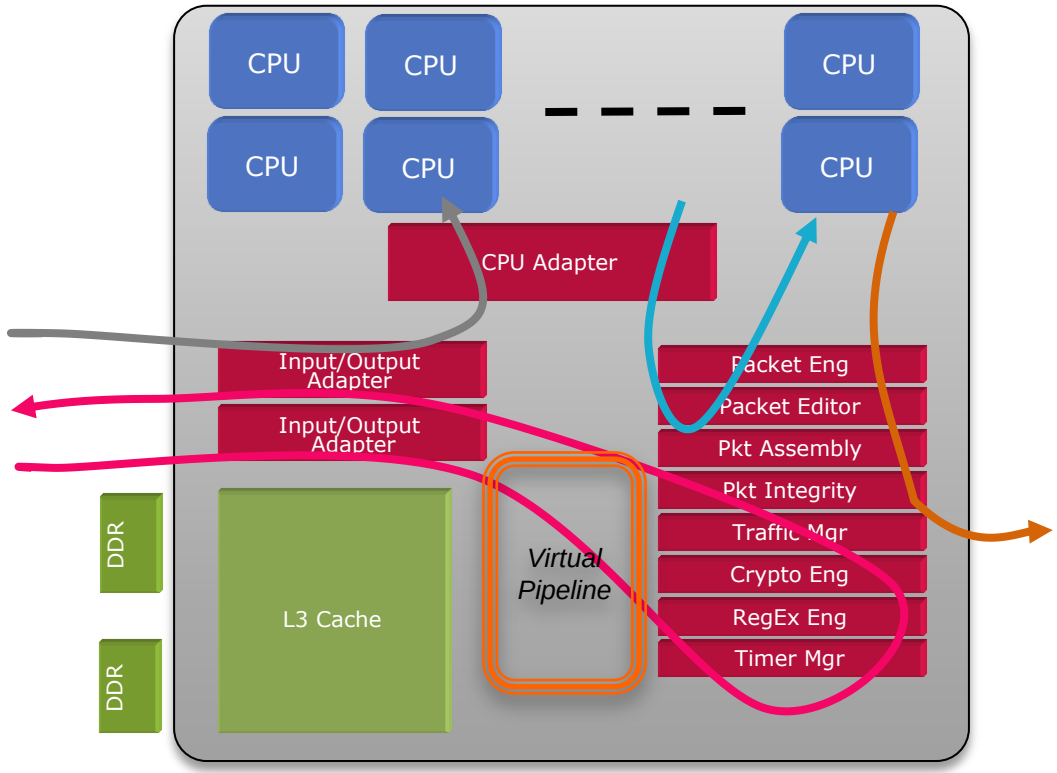
Multicore Axxia Usage Models

Pre-processing

Examples
One or more of:
- Stateful Classification
- TCP assist/offload
- Rate shaping
- Crypto (eg, IPsec / Kasumi/Snow3G)
- IP de-fragmentation

Fast Path Processing

Examples
- Ethernet Switching
- IPv4/v6
- IPsec
- Protocol Interworking
- Wireless transport



Intra-processing

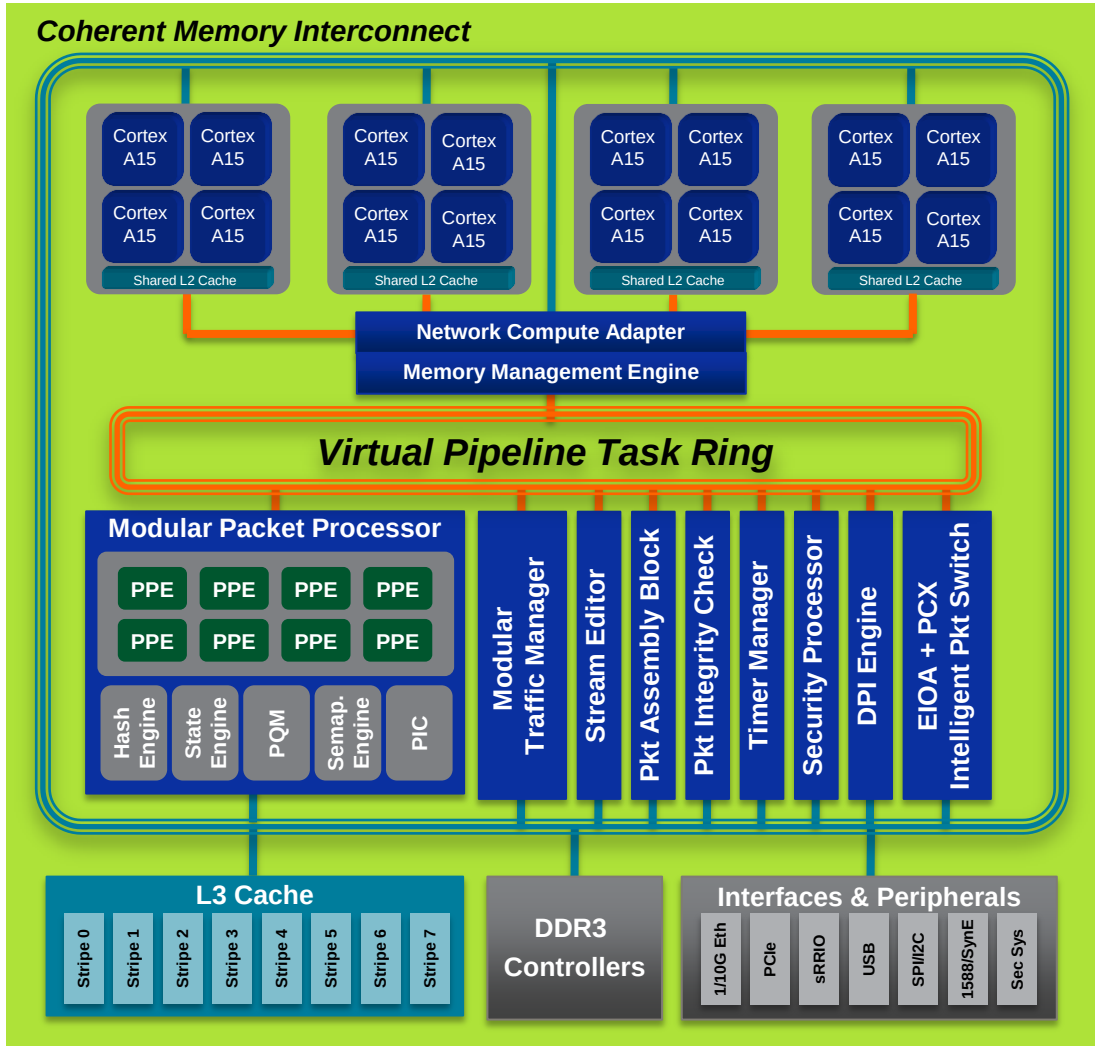
Examples
One or more of:
- RegEX Offload
- Crypto Offload
- Scheduler/shaping
- Checksum/CRC generation

Post-processing

Examples
One or more of:
- Traffic Management
- Crypto Offload
- Scheduler/shaping
- Checksum/CRC generation
- IP fragmentation
- Multi-cast

AXXIA provides more powerful and more flexible acceleration
compared to other multicore architectures

Axxia 5516: Industry Leading Innovation



First High-End 16 Core ARM Multicore Communication Processor

First Fully Cache Coherent ARM CCN-504 Network Interconnect

Market Leading Acceleration Engines and Packet Processing

First Integrated Ethernet Switch with 16 10Gb Ethernet links

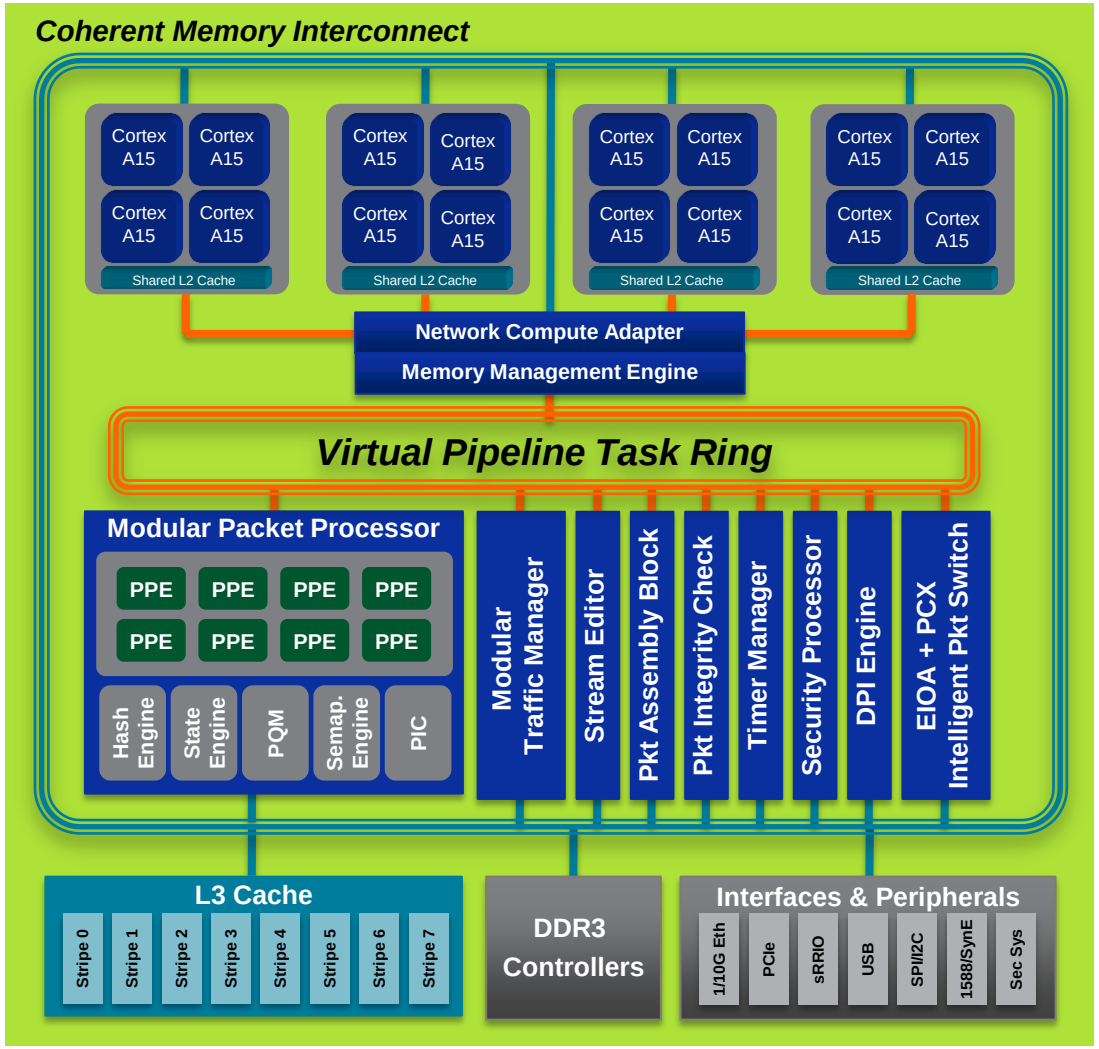
Samples Delivered on Schedule with customer Linux bring-up in 2 days

AVAGO TECHNOLOGIES

ARM

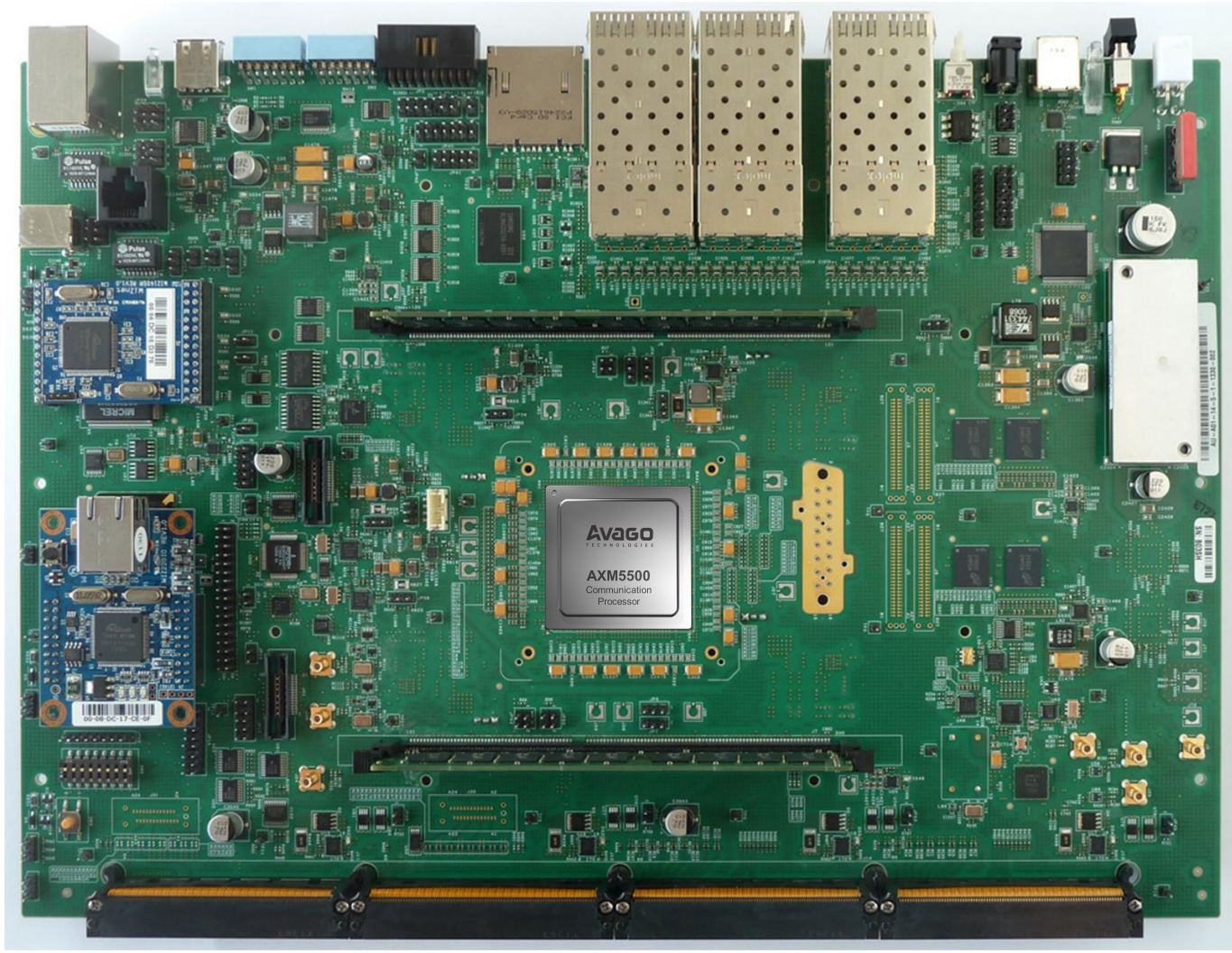
AXM5516 Product Overview

- **Compute Complex System**
  - Up to 16x ARM Cortex A15 cores
  - 3.5DMIPS/MHZ/Core
  - Up to 1.6GHz per core
  - 2MB L2 per 4 core cluster
  - 8MB Shared non-inclusive L3 Cache
  - 16-Core SMP support - HW coherency
  - Hardware Virtualization Support
- **Memory Subsytem**
  - 2x 72 DDR3
- **Secure System Complex**
  - Including secure boot, parameter storage & long-term data storage
  - Boundary interface protection features
- **System Communication**
  - Virtual Pipeline™
- **Network Compute Adapter**
  - CPU connection to virtual pipeline
  - Support flexible flow aware load balancing, ordered and atomic functionality
  - Same connection to on chip cores and external cores over PCI-E/SRIO
  - Easily adaptable to future cores
- **Acceleration Engines**
  - Packet Processing (50Gbps)
  - Security Engine (20Gbps)
  - DPI Engines (7Gbps)
  - Non-blocking L2 switching for Ethernet
  - Trafifc Manager (Flexible 7 layer hierachy, millions of queues & schedulers, 25Gbps)
  - Timer Manager (millions of timers)
- **Flexible SerDes Interfaces**
  - Up to 16x 10GbE via XFI / SFI / 10GBaseKR
  - Up to 8x GbE via QSGMII
  - Up to 20x GbE via SGMII
  - 2 controllers PCIe Gen2
  - 2 controller SRIO v2.2
- **Miscellaneous**
  - USB, UART, I2C, SPI, GPIO
  - 1588 & SyncE Support
  - Secure Boot & System Features
- **Technology**
  - 28nm Technology
  - Samples delivered Q3 2013



AXM5516 Evaluation & Test Board

- Used internally and by cutomers
- Linux and test applications up and running on board very quickly after first silicon
- DIMM based DDRs for flexible test configs
- Advanced Mezzanine Card (AMC) based connectivity
  - Up to16x 10Gbe
  - Up to 20x Gbe
  - SRIO/PCI
  - USB
- SyncE and timing protocol (e.g. IEEE 1588) support
- Full debug/JTAG connectivity
- Power measurement capability
  - Measure power under actual application load and conditions, not just best case

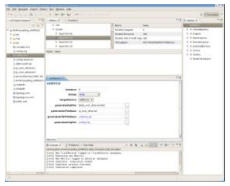


AVAGO TECHNOLOGIES

ARM

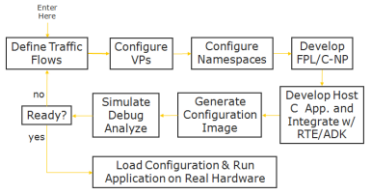
Axxia Software & System Solutions

ASE



Development Tools
- Compilers &Source level Debuggers
- Full Chip Simulation & Debug Environment
- JTAG based debuggers from 3rd parties

RTE



Device API
- Configuration
- Management
- Diagnostics

ADK

IEEE IETF ITU MEF

Application Enabling Software
- Wireless transport & chaining
- Mobile backhaul
- Aggregation

Reference Systems & SW

Reference & Evaluation Systems & Software
- Development & Emulation Platforms
- AMC,ATCA production boards
- Reference Linux BSP, Uboot

3rd Party

QOSMOS tieto.com WIND ARICENT

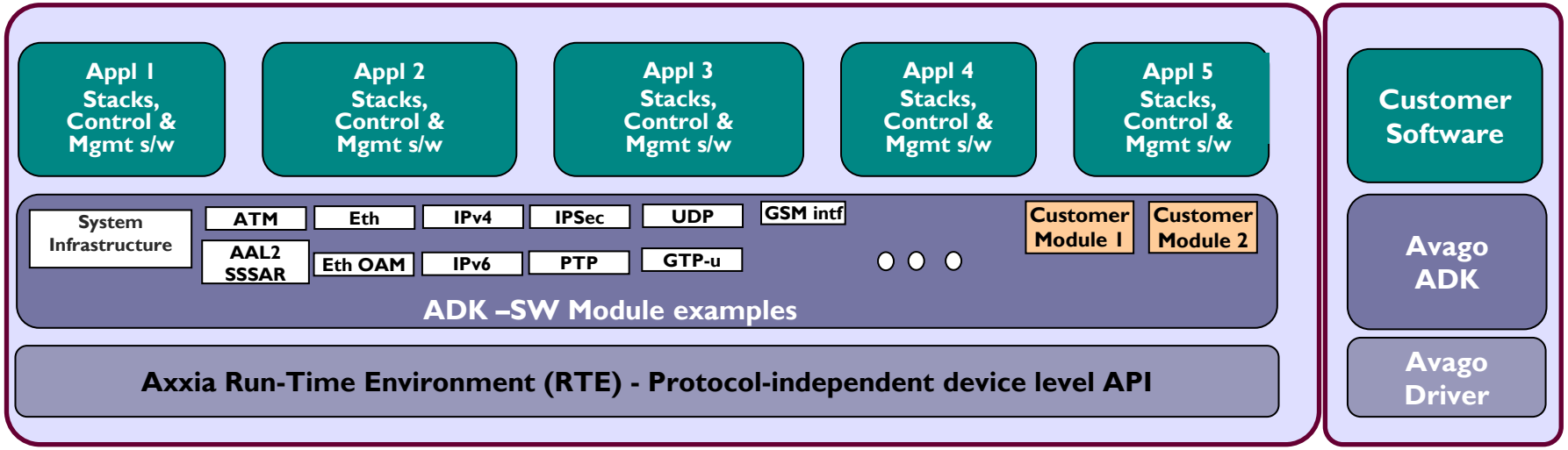
Partner Services
- Software Development
- System Integration & Verification
- Life-time management

Robust Software & Development Tool Offering

AVAGO TECHNOLOGIES

ARM

Axxia Application Development Kit (ADK)



- **Avago offers a comprehensive suite of SW**
  - ✓ADK provides simple method to leverage power of virtual pipeline
  - ✓Fastpath leverages Virtual Pipeline accelerations for very high performance
  - ✓Customers can mix and match modules as needed for their application
  - ✓Device independent C-API at functional level of abstraction simplifies s/w integration
  - ✓API consistent across entire Axxia family
  - ✓Architecture and framework s/w supports addition of customer-proprietary modules

Low Cost, Rapid System Development
Differentiation, Scalable and Future Proof Deployments

AXXIA 5516 For Networking Applications

- World's first cache-coherent, 16 core SMP ARM-based processor
- Based on flexible AXXIA multicore SoC architecture
- Built with ARM CCN-504 interconnect and Cortex-A15 processors
- Industry leading acceleration
- Virtual Pipeline™ acceleration interconnect
- Full software solution including Application Development Kit (ADK)

Summary

- ARM is enabling unique solutions across the enterprise space with ground-breaking CPU and system IP
- ARM's strength is in its ecosystem and in strong relationships with partners such as Avago
- Avago Axxia platform architecture offers industry-leading performance and power-efficiency
- Axxia 5516: innovative Avago capabilities supported by ARM IP for enterprise

Thank you.